



IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

INVENTORS:

Thomas J. Krutsick

CASE: 5

EXPRESS MAIL

These papers are being deposited
as EXPRESS MAIL with the
US POST OFFICE addressed to:
ASSISTANT COMMISSIONER
FOR PATENTS, WASHINGTON
D.C., 20231 by [Signature]
date February 3, 2003
EM# EU194048705US

TITLE: FIELD PLATED RESISTOR WITH ENHANCED
ROUTING AREA THEREOVER

SERIAL NO. 09/650,604

GROUP ART UNIT 2826

FILING DATE 04/18/00

EXAMINER AHMED N. SEFER

THE COMMISSIONER OF PATENTS AND TRADEMARKS
WASHINGTON, D.C. 20231

SIR:

In response to the Office action mailed 10/01/02 please amend the above
referenced application as follows:

In the claims:

Please amend claim 28 to read:

28. An integrated circuit having a field-plated resistor the field-plated
resistor comprising:

a resistor body formed in a semiconductor substrate, the
resistor body having first and second contact regions,